SAMSUNG

SIEMENS

A Novel Solution for 3nm/4nm and Below LVS Challenges: Local Layout Effects Extraction QA in LVS Rule Deck

AUTHORS:

JAEYOUNG SO(1), JIMIN YEO(1), JONGKU KANG(1), HEEJAE LIM(1), YONGSEOK LEE(1), MINHO JUNG(1), YOUNGROG JO(1)

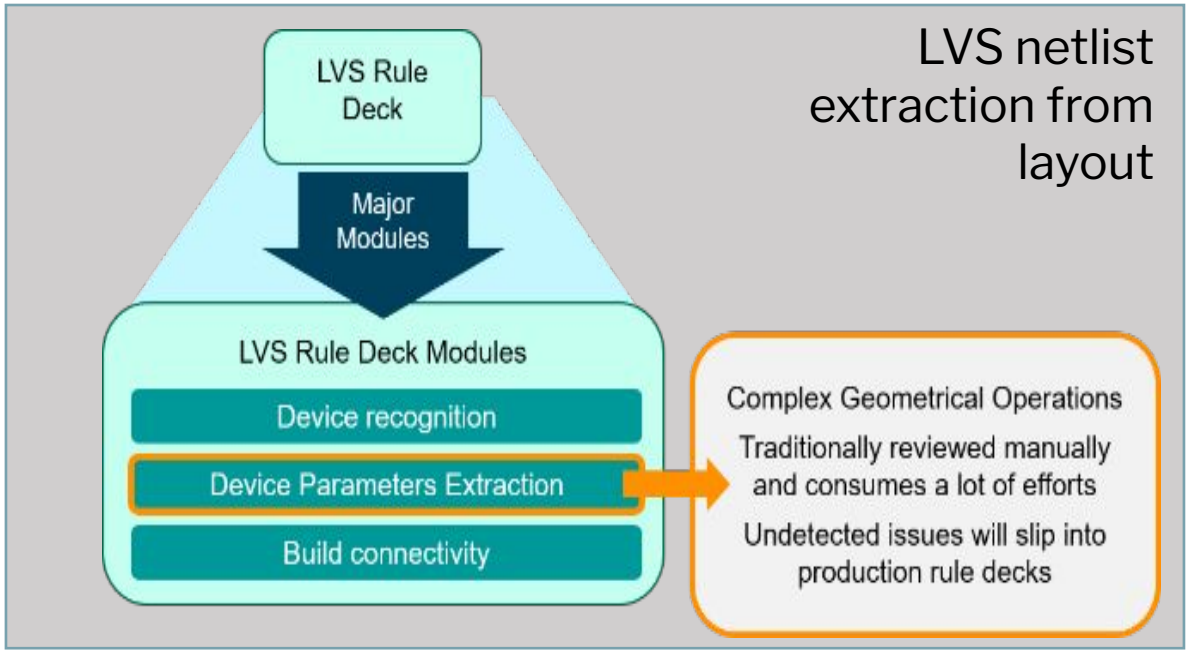
AHMED SALEH(2), MOHAMED ALIMAM(2)

(1) **SAMSUNG ELECTRONICS**

(2) **SIEMENS EDA**

Introduction

- A Process Design Kit (PDK) models a fabrication process of the foundry and is used by the foundry customer to create, simulate, and verify product designs before fabricating the products using the foundry's process.
- A critical step in the design flow of foundry customers is to verify that the electrical behavior of designs before and after layout development is consistent.
- In advanced technology nodes such as 3nm/4nm and below, Local Layout Effects (LLE) have a significant impact on device performance.
- Accurately modeling these effects is essential for ensuring the correct functionality of the circuit. However, the manual effort required to qualify LLE parameters at such nodes is extensive, making it impractical to perform the task manually. To overcome this challenge, we propose an automatic solution for qualifying LLE parameters in the LVS (Layout vs. Schematic) rule deck.



LVS (Layout vs. Schematic) netlist extraction from layout

Motivation
Accurate Accounting for **L**ocal **L**ayout **E**ffects (LLE) on Circuit Simulations

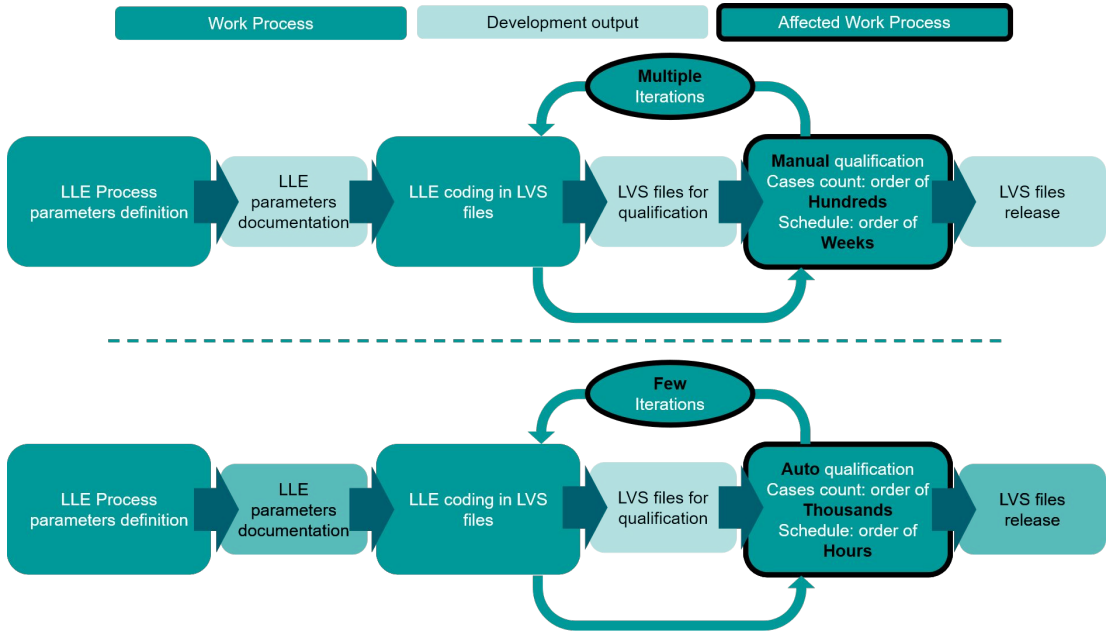
- In advanced technologies the behavior of devices changes according to their **layout context**.
- Before the layout is completed, designers simulate their designs using netlists that are **unaware** of the layout context.
- After the layout of the design is finalized, verification of the design behavior **before and after** layout is critical to ensure the design yield.
- **Correct extraction of Local Layout Effects (LLE) is critical for the electrical yield of designs in advanced semiconductors manufacturing.**
- The LVS Rule Deck is the technology file responsible for extracting local layout effects parameters.

Technology node (nm)	18	14	11	8	7	5	4	3	2
LLE parameters count	1x	2.1x	2.1x	6.4x	7.7x	8x	8x	8.4x	8.6x

LLE parameters count vs technology node

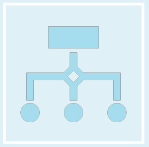
Methodology
A novel solution involves automatic qualification of LLE parameters in the LVS rule deck

- LLE Checker tool is used to extract local layout effects and offers intelligent methods for simplified debugging.
- The benefits of the LLE checker can be understood by contrasting the release process of the LVS rule files before and after the introduction of the LLE Checker.
- The key issue that was resolved by the LLE Checker is the ability to qualify thousands of test cases in an automated flow that produces compact and easy to debug results files.



LVS rule file release process for the LLE parameters section. Top flow is the traditional flow where manual verifications led to slow discovery of issues and long iterations before release. At the bottom is the release process utilizing the LLE checker

Methodology
A novel solution involves automatic qualification of LLE parameters in the LVS rule deck



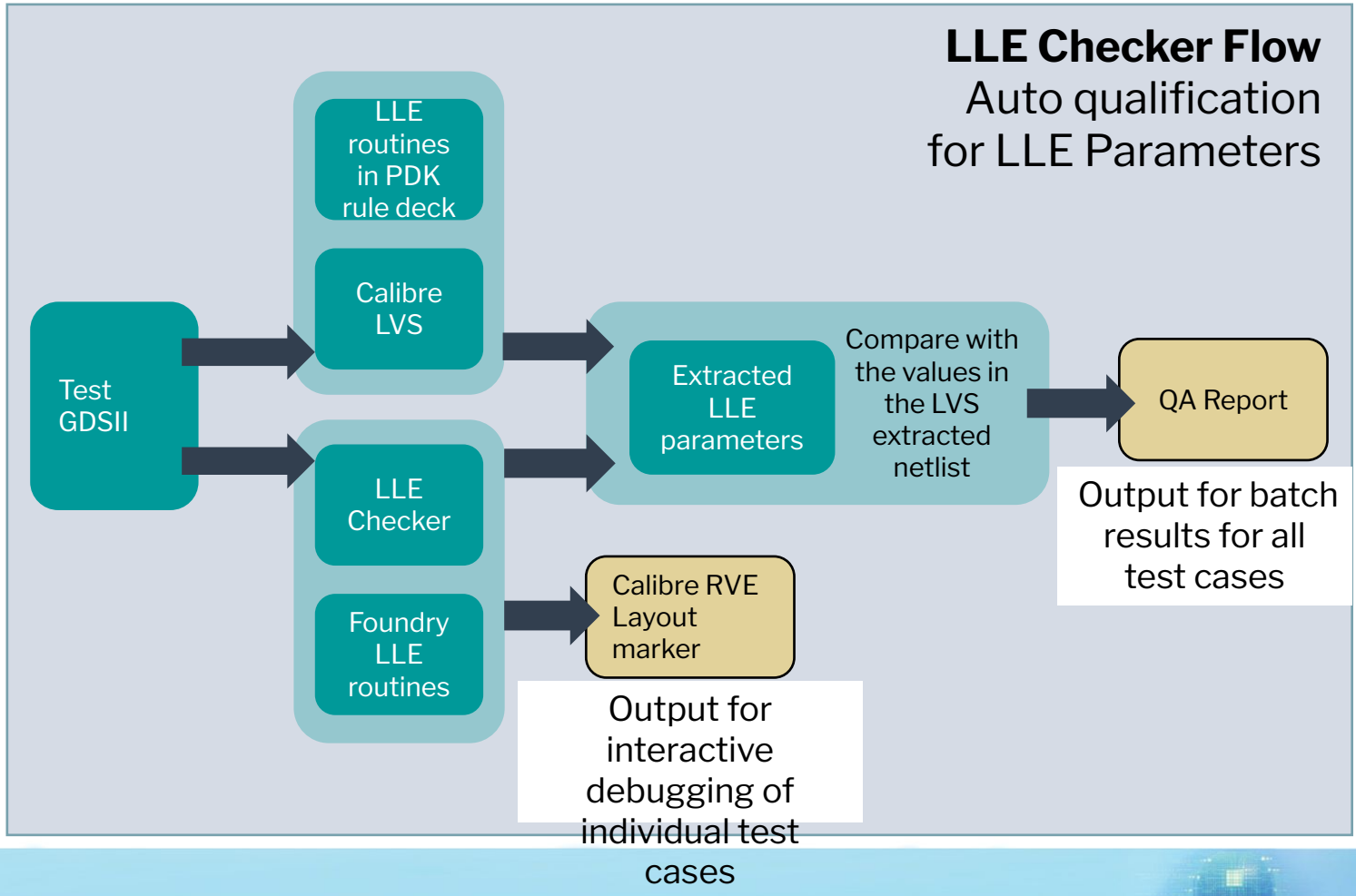
In the qualification flow, outputs from the Calibre LVS and LLE checker are compared.

If the results match (pass), then the confidence that the result is correct for both is high.

If there is a mismatch (fail), the qualification engineer can easily debug using the marker layers to check how the parameter in question was computed.

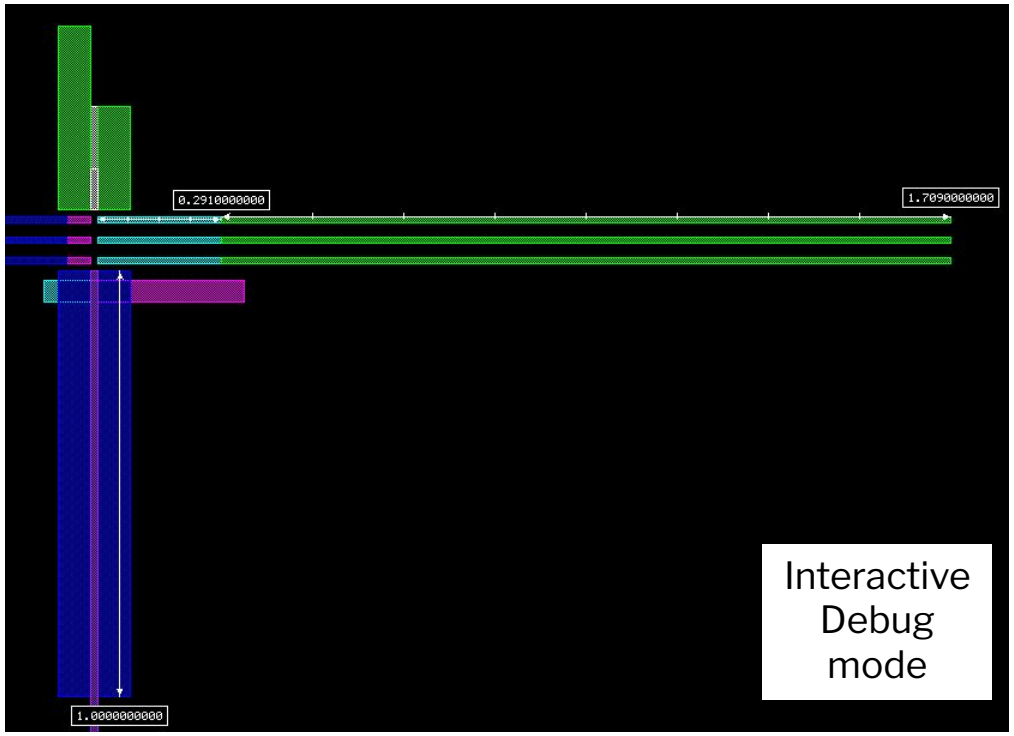
Main Idea
Auto Qualification of LLE Parameters in the LVS Rule Deck on STD Cells and Foundation IP

- The manual effort required for full qualification of LLE parameters at 2nm can be estimated using the formula below, which is derived from real data numbers.
- Number of LLE parameters ~ 10's of parameter per fet
- Number of test cases to verify ~ 2000
- Number of devices per test case ~ 10
- Inspection time for one parameter in one device is ~1min of engineering time.
- Total verification time needed is ~ (10's of parameter per fet) x 2000 x 10 x 1min which is well over thousands of engineering hours.
  - **Manual qualification is not Possible;**
    - **An Automatic solution is needed.**



Main Idea
Easy Debug for Millions of Qualification Test Cases

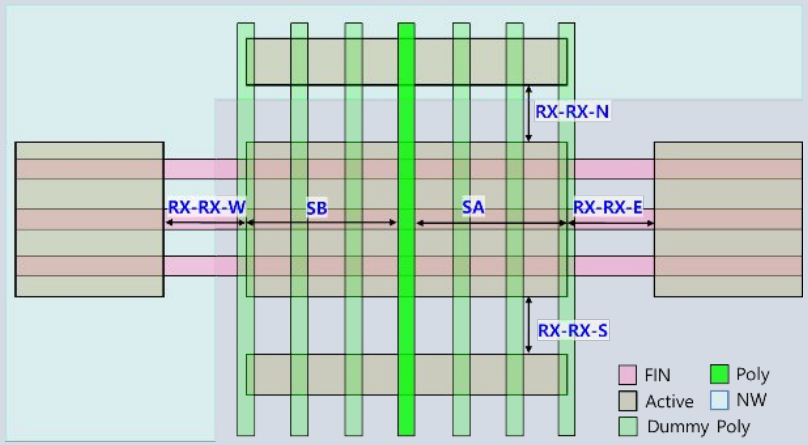
- LLE checker provides output marker layers; Using Calibre RVE, the user can view on the input layout to show exactly how each parameter was computed:
  - LLE SA
    - The distance between the right gate edge to the edge of RX layer measured on the Fin layer. Highlighted in cyan color.
  - LLE RX-RX E
    - The distance between the right RX edge layer containing the gate and the nearest left RX edge measured along the Fin layer. Highlighted in green.
  - LLE RX-RX S
  - The distance between the bottom RX edge containing the gate and the nearest top edge of RX layer measured along the poly direction. Highlighted in blue.



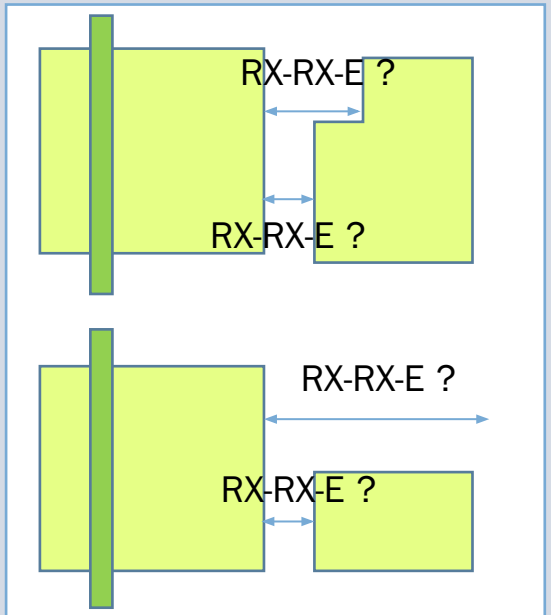
Batch mode

M1	sa	CDL	291.0	Layout	291.0	Pass
M1	rxrxe	CDL	1709.0	Layout	1709.0	Pass
M1	rxrxs	CDL	1000.0	Layout	1000.0	Pass

Evidence
Impact of LLE on Device Performance (RX-RX Example)

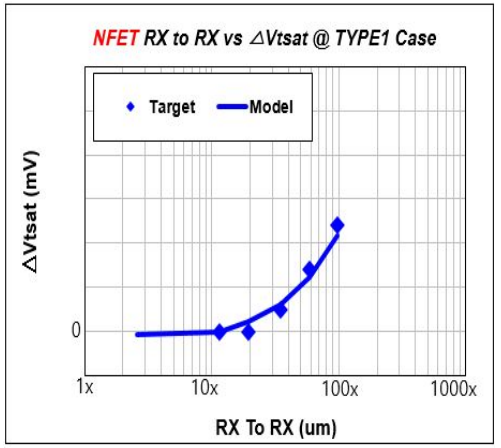


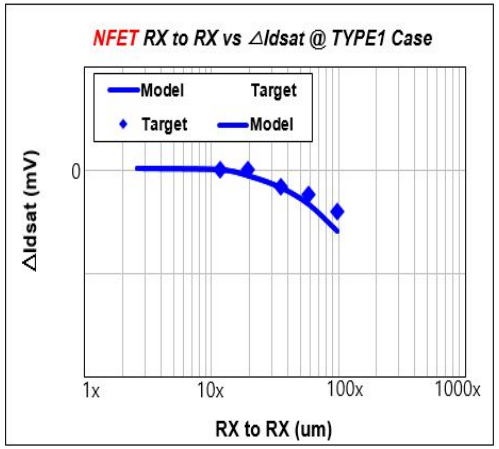
RX-RX **Specification**: The distance between the Active well of the transistor and adjacent Active wells in all four directions: East (RX-RX-E), West (RX-RX-W), North (RX-RX-N). And South (

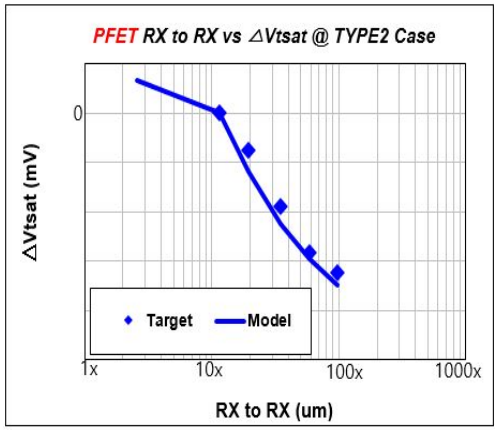


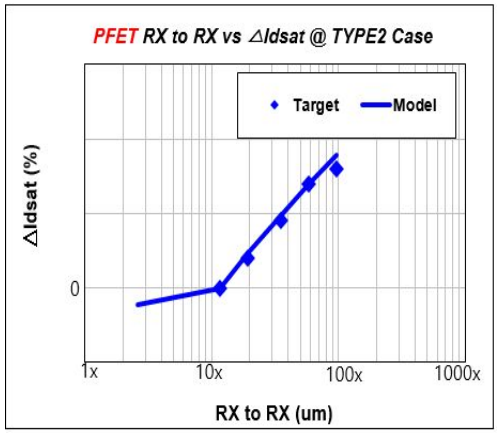
Examples of Corner Cases that needs to be qualified for RX-RX-E

Corner cases not explicitly defined in specifications but can occur in design data.









Variation in MOS electrical behavior vs variation in LLE RX-RX values. Top row and bottom row are for 2 different transistors.

Results
Enabled Qualification on STD Cell Library and Foundation IPs

LLE Checker was used to qualify the technology's standard cell library, and foundry IP. The test cases count per technology is in the order of thousands. LLE Checker enabled checking millions of cases per technologies with only a few hours of runtime.

Using LLE Checker improved the quality of LVS LLE and guaranteed accurate calculation over millions of cases.

The introduction of LLE checker has dramatically reduced verification time. (> ~1e4 times reduction)

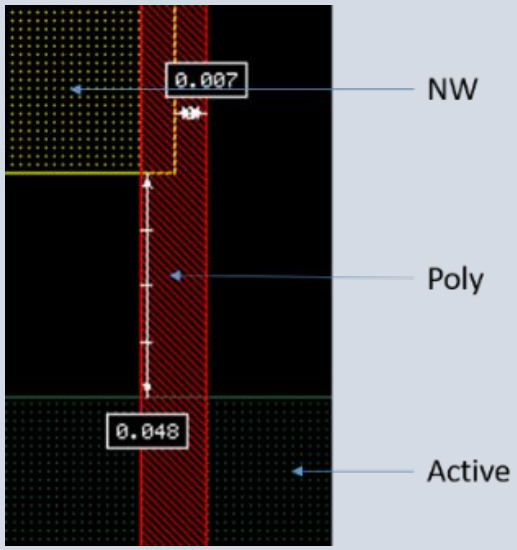
Technology Node	Total number of cases checked	Runtime of all test cases with LLE Checker (hours)	Estimated manual time (hours)
A	1,458,540	3.16	24,309
B	4,715,040	4.86	78,584
C	11,627,430	12.58	193,791
D	1,102,000	0.26	18,367
E	3,185,070	0.67	53,085
F	2,924,784	0.84	48,746
G	17,712,000	3.35	295,200
H	2,392,320	2.36	39,872
I	88,784	0.18	1,480

Results
Ability to qualify test cases, resolving key issues in the release process of LVS rule files

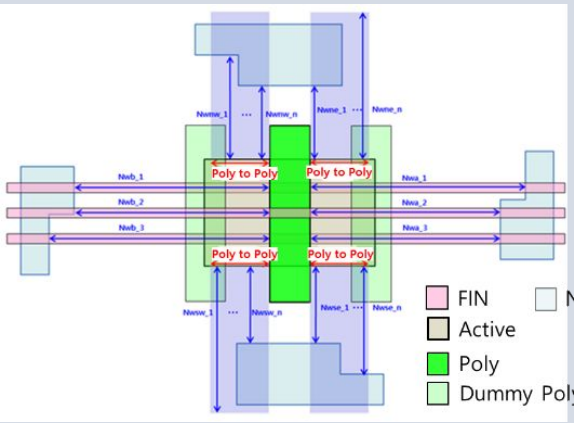
- Thorough verification of LLE routines across thousands of cases was not possible by manual work, making the LLE Checker an essential tool for increasing code quality and confidence.

- Interesting findings were discovered when testing across thousands of test cases, including issues with layout configurations not covered by LLE parameter specifications.

- One case where this occurred was with LLE NWN (distance from gate to north NWELL) , which was redefined to account for NWELL corners above the gate that were not considered in the original specification.



Layout snapshot for LLE NWN showing a corner case not covered by the specifications



LLE_NWN updated specification

Future Work

- As semiconductor technology nodes continue to shrink, local layout effects are becoming increasingly important to model accurately.
- Moving forward, there are several potential directions for future work.
  - Firstly, further refinement and optimization of the LLE Checker tool can be pursued, with a focus on reducing runtime and improving accuracy. Additionally, expanding the tool's capabilities to cover more advanced LLE effects and extending its use to other parts of the design flow may be explored.
  - Furthermore, the use of machine learning and artificial intelligence techniques to enhance LLE modeling and verification is another promising area for future research.
  - Finally, the collaboration between foundries and EDA tool vendors can be strengthened to jointly develop solutions that address the challenges posed by advanced technology nodes.

Summary

- **Objective:**
  - The LLE Checker tool presented in this work provides an automated solution for qualifying LLE parameters in the LVS rule deck, enabling the thorough verification of LLE routines across thousands of test cases.
  - LLE Checker enabled Qualification on STD Cell Library and Foundation IPs.
- **Challenges:**
  - During the LLE process definition phase, a lot of simulations on different layout configurations needs to be done to derive the LLE definition for each parameter.
  - Iterations and coverage of different layout structure can be engineering intensive.
- **Success:**
  - Moving LLE Checker from the LVS files qualification phase to be used early during process parameters definition will further improve coverage of the LLE specifications as shown by the LLE NWN example and the turnaround time of the entire process.
  - The test cases count per technology is in the order of thousands. LLE Checker enabled checking millions of cases per technologies with only a few hours of runtime.
  - Using LLE Checker improved the quality of LVS LLE and guaranteed accurate calculation over millions of cases.
  - The introduction of LLE checker has dramatically reduced verification time. (> ~1e4 times reduction).